What Is Claimed Is:

1. A method of forming a bit line contact structure, comprising:

providing a substrate with a transistor including a gate electrode and a source/drain region thereon, the gate electrode being protected with a first insulating layer;

conformally forming a titanium layer on the substrate with the transistor thereon;

conformally forming a titanium nitride layer on the titanium layer;

conformally forming a tungsten layer on the titanium nitride layer;

defining the tungsten layer, the titanium nitride layer and the titanium layer to form an inner landing pad on the source/drain region;

conformally forming a passivation layer on the inner landing pad, the transistor and the substrate;

forming a second insulating layer with an even surface on the passivation layer;

forming a contact hole in the second insulating layer and the passivation layer to expose the inner landing pad; and

filling a metal material in the contact hole.

2. The method of claim 1, wherein a thickness of the tungsten layer is 200-400 Å.

3. The method of claim 1, wherein the tungsten layer is defined by dry etching.

4. The method of claim 3, wherein the tungsten layer is dry etched with $Cl_2/F_2/O_2$.

5. The method of claim 1, wherein the tungsten layer is defined by wet etching.

6. The method of claim 5, wherein the tungsten layer is wet etched with APM solution (NH_4OH-H_2O_2-H_2O) at about 40°C.

7. The method of claim 1, wherein the passivation layer comprises silicon nitride.

8. The method of claim 1, wherein the passivation layer has a thickness of 110-130 Å.

9. The method of claim 1, wherein the second insulating layer is a BPSG/TEOS stacked layer.

10. The method of claim 1, wherein a method of forming a BPSG layer of the BPSG/TEOS stacked layer comprises:

depositing a material of BPSG on the passivation layer; and

polishing the material of BPSG until a part of the passivation layer is exposed.

11. The method of claim 10, wherein the BPSG layer of the BPSG/TEOS stacked layer has a thickness of 5900-7300 Å, and a TEOS layer of the BPSG/TEOS stacked layer has a thickness of 3600-4400 Å.

12. The method of claim 1, wherein the metal material filled in the contact hole is tungsten.

13. A method of forming a bit line contact structure on a substrate having a memory array region and a logic circuit region and having a transistor including a gate electrode and a source/drain region thereon, the gate electrode protected with a first insulating layer, the method comprising:

conformally forming a titanium layer on the substrate with the transistor thereon;

conformally forming a titanium nitride layer on the titanium layer;

conformally forming a tungsten layer on the titanium nitride layer;

defining the tungsten layer, the titanium nitride layer and the titanium layer to form an inner landing pad in the memory array region to contact the source/drain region;

conformally forming a passivation layer on the inner landing pad, the transistor and the substrate;

forming a second insulating layer with an even surface on the passivation layer;

forming first, second and third contact holes in the second insulating layer and the passivation layer to expose the inner landing pad in the memory array region, the gate electrode in the logic circuit region and the source/drain region in the logic circuit region respectively; and

filling a metal material in the first, second and third contact holes.

14. The method of claim 13, wherein a thickness of the tungsten layer is 200-400 Å.

15. The method of claim 13, wherein the tungsten layer is defined by dry etching.

16. The method of claim 15, wherein the tungsten layer is dry etched with $Cl_2/F_2/O_2$.

17. The method of claim 13, wherein the tungsten layer is defined by wet etching.

18. The method of claim 17, wherein the tungsten layer is wet etched with APM solution (NH_4OH-H_2O_2-H_2O) at about 40°C.

19. The method of claim 13, wherein the passivation layer comprises silicon nitride.

20. The method of claim 13, wherein the passivation layer has a thickness of 110-130 Å.

21. The method of claim 13, wherein the second insulating layer is a BPSG/TEOS stacked layer.

22. The method of claim 21, wherein a method of forming a BPSG layer of the BPSG/TEOS stacked layer comprises:

depositing a material of BPSG on the passivation layer; and

polishing the material of BPSG until a port of the passivation layer is exposed.

23. The method of claim 22, wherein the BPSG layer of the BPSG/TEOS stacked layer has a thickness of 5900-7300 Å, and a TEOS layer of the BPSG/TEOS stacked layer has a thickness of 3600-4400 Å.

24. The method of claim 13, wherein the metal material filled in the first, second and third contact holes is tungsten.

25. A bit line contact structure, comprising:

a substrate;

a transistor on the substrate, the transistor including a gate electrode and a source/drain region, the gate electrode protected with a first insulating layer;

an inner landing pad on a surface of the transistor and the source/drain region, the inner landing pad comprising a conformal titanium/titanium nitride/ tungsten stacked layer from the bottom up;

a passivation layer on the transistor and the substrate;

a second insulating layer with an even surface on the passivation layer;

a contact plug in the second insulating layer and the passivation layer to contact the inner landing pad; and

an interconnecting landing pad on the contact plug.

26. The bit line contact structure of claim 25, wherein a thickness of the tungsten layer of the inner landing pad is 200-400 Å.

27. The bit line contact structure of claim 25, wherein the passivation layer comprises silicon nitride.

28. The bit line contact structure of claim 27, wherein the passivation layer has a thickness of 110-130 Å.

29. The bit line contact structure of claim 27, wherein the contact plug and the interconnecting landing pad comprises tungsten.